Rising Stars in Computer Architecture (RISC-A) Workshop 2018

Date: October 5th, 2018
Time: 9 AM - 5:30 PM
Location: Marcus Nanotechnology Building: 1
Rooms 1117-1118
WELCOME TO RISC-A @ GEORGIA TECH!

- What is RISC-A?
- Format
- Selection Process
- Invited Speakers
- Agenda for Today
- Logistics
WHAT IS RISC-A?

- Forum bringing together top graduating PhD/post-doc students working in computer architecture looking for academic positions
  - Scientific and Technical Discussions
    - Learn about the breadth of top research across computer architecture
  - Informal discussions about navigating academia

- Intended Purpose: For the Invited Speakers
  - Early prep to get your application package ready
  - Practice a potential job talk in an informal yet realistic setting
    - Audience of senior faculty, junior faculty, and students from ECE and CS
  - Interact with and get feedback from faculty and students at GT
  - Ask questions – I am sure you have many - about life in academia
    - from how to get there to what to do once you get there
  - Mentorship -- Learn about each other and from each other

- Intended Purpose: For Georgia Tech faculty and students
  - Interact with our future peers – you are going to be our future colleagues and collaborators, wherever you end up joining
  - Learn about the top graduating students who intent to be on the academic market and their research
Inspiration: Sister Initiatives
- Rising Stars in EECS – for women in academia
- Cornell’s ORIE Workshop

Scope: Broad vs Narrow
- Something too broad (say ECE or CS wide) makes it harder to have focused discussions
  - Both technical and non-technical
- Limited to Domain of Computer Architecture
  - Quite broad – from software (applications/OS/compiler) to hardware (architecture/microarchitecture/circuits/devices)
  - How we defined “Computer Architecture”? → Target conferences for publications and attendance

Why RISC?
- A forum to mentor Rising Stars in Computing (RISC) seemed more appropriate than inviting Continuing Stars in Computing (CISC) 😊
**SELECTION PROCESS**

- **RISC-A 2018 Co-Chairs:** Tushar Krishna & Moin Qureshi

- **Solicited Applications from graduating students/post-docs**
  - Flyers at ISCA (June 2018)
  - Emailed announcements to colleagues at US and International universities

- **Application Format [Due August 31<sup>st</sup> 2018]**
  - CV
  - Research Statement
  - Letter of Recommendation from Advisor(s)

- **Number of Applications Received:** 13

- **Selection Criteria**
  - Research Contributions
    - Papers in top-tier venues, 1<sup>st</sup> author papers
  - Advisor Recommendation
  - Research Statement
SELECTED CANDIDATES

Raghav Pothukuchi
UIUC

Ashay Rane
Univ of Texas at Austin

Brandon Reagen
Harvard/Facebook

Chris Torn
Cornell

Nandita Vijaykumar
CMU

Mengjia Yan
UIUC
# Agenda for Today

<table>
<thead>
<tr>
<th>Time</th>
<th>Agenda</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>9 - 9:30</td>
<td>Coffee + Breakfast</td>
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<tr>
<td>9:30 - 9:40</td>
<td>Welcome by Workshop Chairs</td>
<td>Tushar Krishna and Moin Qureshi</td>
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<td>9:40 - 9:50</td>
<td>Welcome by ECE</td>
<td>Justin Romberg (Associate Chair for Research, School of Electrical and Computer Engineering)</td>
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<td>9:50 - 10:00</td>
<td>Welcome by SCS</td>
<td>Lance Fortnow (Chair, of School of Computer Science)</td>
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<td>10 - 10:45</td>
<td>Mengjia Yan (UIUC)</td>
<td>Secure Processor Hardware</td>
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<td>10:45 - 11:30</td>
<td>Ashay Rane (UT Austin)</td>
<td>Broad-Based Side-Channel Defenses for Modern Processor Architectures</td>
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<td>11:30 - 12:30</td>
<td>Panel Discussion</td>
<td>Topic: Life in Academia - A View from the Other Side.</td>
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<tr>
<td>11:30 - 12:30</td>
<td>Panel Discussion</td>
<td>Panelists: Vivek Sarkar, David Devecsery, Hyesoon Kim, Saibal Mukhopadhyay</td>
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<td>12:30 - 1:45</td>
<td>Lunch (Catered)</td>
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<td>1:45 - 2:30</td>
<td>Raghavendra Pothukuchi (UIUC)</td>
<td>Extreme-Efficiency Computing</td>
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<td>2:30 - 3:15</td>
<td>Nandita Vijaykumar (CMU)</td>
<td>Expressive Memory: Rethinking the Hardware-Software Contract with Rich Cross-Layer Abstractions</td>
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<td>3:15 - 3:30</td>
<td>Break</td>
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<td>3:30 - 4:15</td>
<td>Christopher Torng (Cornell)</td>
<td>Software, Architecture, and VLSI Co-Design for Task-Based Parallel Runtimes</td>
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<td>4:15 - 5:00</td>
<td>Brandon Reagen (Harvard/Facebook)</td>
<td>On the design and optimization of hardware accelerators with applications in deep learning</td>
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<td>5:00 - 5:10</td>
<td>Closing Remarks</td>
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<td>5:30 - 7:30</td>
<td>Dinner Banquet @ King &amp; Duke</td>
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LOGISTICS

- WiFi for Visitors:
  - GTvisitor

- Agenda and Talk Abstracts:
  - [http://risca.gatech.edu](http://risca.gatech.edu)

- Food and Coffee
  - At the back of the room
CONCLUDING REMARKS

- To all attendees (visitors and local):
  - Keep the sessions interactive

- Maintain a friendly and informal atmosphere
  - This is NOT a technical conference
  - This NOT an interview
  - Use this opportunity to get and give honest feedback

- For those on the edge between academia and industry
  - Use this opportunity to understand trade-offs
  - We love our jobs in academia. Ask us why? 😊

- Welcome once again to the Inaugural Rising Stars in Computer Architecture Workshop 2018 at Georgia Tech!
  - Looking forward to an exciting day ahead!